

CLAIMS

What is claimed is:

- 1 1. A computer system comprising a microprocessor having a dynamically
2 re-configurable trace cache to provide application specific configuration of the
3 trace cache.
- 1 2. The computer system of claim 1 wherein the trace cache comprises:
2 a tag array;
3 a data array; and
4 a next fetch address (NFA) array.
- 1 3. The computer system of claim 2 wherein the tag array, the data array and
2 NFA array each store one or more fetch address entries and one or more
3 temporal address entries.
- 1 4. The computer system of claim 3 wherein each trace stored in the trace
2 cache is assigned an index value.
- 1 5. The computer system of claim 4 wherein the tag array, the data array and
2 the NFA array each comprise a decoder to access a trace stored in the one or
3 more temporal address entries using an index value.
- 1 6. The computer system of claim 3 wherein the one or more temporal
2 address entries are generated by simulating to identify dynamic traces, the

3 execution behavior of the dynamic traces and generating an index value for each
4 identified trace.

1 7. A method comprising: ✓
2 generating an index value to be associated with a first instruction trace;
3 storing the first trace within a first of a plurality of cache array entries
4 using an index value associate with the first trace; and
5 retrieving the first trace from the first cache array entry using the index
6 value associated with the first trace.

1 8. The method of claim 7 further comprising storing a second instruction
2 trace within the plurality of cache array entries using a fetch address if there is no
3 index value associated with the second trace.

1 9. The method of claim 8 further comprising retrieving the second trace from
2 the plurality of cache array entries using the fetch address.

1 10. The method of claim 7 further comprising:
2 simulating a trace cache to identify the execution behavior of the first
3 trace; and
4 attaching the index number to a branch instruction that forms the first
5 trace.

1 11. The method of claim 7 wherein generating an index value comprises:

2 collecting profile information on traces that are to be generated; and
3 generate indexes for each of the traces.

1 12. The method of claim 11 wherein collecting profile information comprises:
2 recording a fetch address and path number for each of a plurality of
3 fetched traces; and
4 identifying traces that are frequently executed.

1 13. The method of claim 12 further comprising generating a temporal
2 relationship graph for the frequently executed traces, the temporal relationship
3 graph indicating a temporal relationship between two or more of the frequently
4 executed traces.

1 14. The method of claim 13 further comprising allocating each of the
2 frequently executed traces to the plurality of cache array entries, wherein traces
3 having temporal relationships are allocated to different cache array entries.

1 15. The method of claim 13 further assigning an index value for each
2 frequently executed trace after generating the temporal relationship graph.

1 16. A microprocessor comprising:
2 an instruction cache to receive and store the micro-operations as cache
3 lines;
4 a trace cache, coupled to the instruction cache, that is dynamically re-

5 configurable using profile information to provide application specific
6 configuration of the trace cache; and
7 an execution core to execute the micro-operations.

1 17. The microprocessor of claim 16 further comprising:
2 a fill unit to form micro-operations; and
3 branch prediction logic.

1 18. The microprocessor of claim 16 wherein the trace cache comprises:
2 a tag array;
3 a data array; and
4 a next fetch address (NFA) array. ✓

1 19. The microprocessor of claim 18 wherein the tag array, the data array and
2 NFA array each store one or more fetch address entries and one or more
3 temporal address entries.

1 20. The microprocessor of claim 19 wherein each trace stored in the trace
2 cache is assigned an index value.

1 21. The microprocessor of claim 20 wherein the tag array, the data array and
2 the NFA array each comprise a decoder to access a trace stored in the one or
3 more temporal address entries using an index value.

1 22. A trace cache comprising:

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2 a tag array;
3 a data array; and
4 a next fetch address (NFA) array;
5 wherein the tag array, the data array and NFA array each store one or
6 more fetch address entries and one or more temporal address entries.

1 23. The microprocessor of claim 22 wherein each trace stored in the trace
2 cache is assigned an index value.

1 24. The microprocessor of claim 23 wherein the tag array, the data array and
2 the NFA array each comprise a decoder to access a trace stored in the one or
3 more temporal address entries using an index value.

1 25. The microprocessor of claim 22 wherein the one or more temporal address
2 entries are generated by simulating to identify dynamic traces, the execution
3 behavior of the dynamic traces and generating an index value for each identified
4 trace.

1 26. A computer system comprising: 
2 a microprocessor having a dynamically re-configurable trace cache to
3 provide application specific configuration of the trace cache;
4 a chipset coupled to microprocessor; and
5 a main memory coupled to the chipset.

3 provide application specific configuration of the trace cache;

4 a chipset coupled to microprocessor; and

5 a main memory coupled to the chipset.

1 27. The computer system of claim 26 wherein the trace cache comprises:

2 a tag array;

3 a data array; and

4 a next fetch address (NFA) array.

1 28. The computer system of claim 27 wherein the tag array, the data array and

2 NFA array each store one or more fetch address entries and one or more

3 temporal address entries.

1 29. The computer system of claim 28 wherein each trace stored in the trace

2 cache is assigned an index value.

1 30. The computer system of claim 29 wherein the tag array, the data array and

2 the NFA array each comprise a decoder to access a trace stored in the one or

3 more temporal address entries using an index value.